

### FPGA architecture to search for accelerated pulsars with SKA

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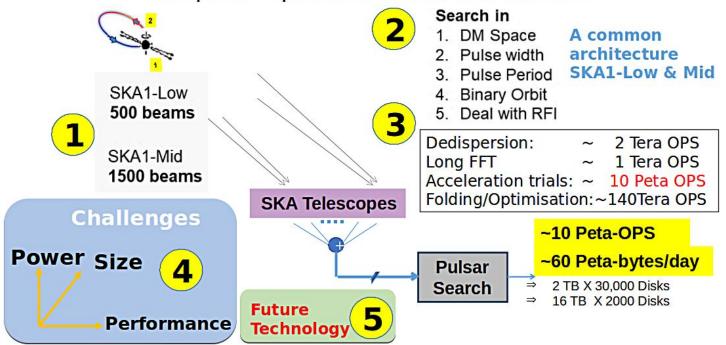
# Outline

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## 1.Introduction

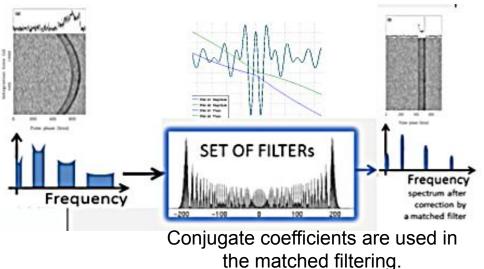
## Pulsar search with SKA

Requires a powerful computing solution



# 2. Design Philosophy

Search for pulsars in binary systems, where the pulse frequency changes significantly during an observation can be undertaken either in a time or frequency domain.



We use frequency domain approach

known as Fourier domain acceleration search (FDAS)

A complex form matched filters used to deaccelerate the input signals A new FPGA architecture developed for FDAS

# 3. Design details - Matched filtering

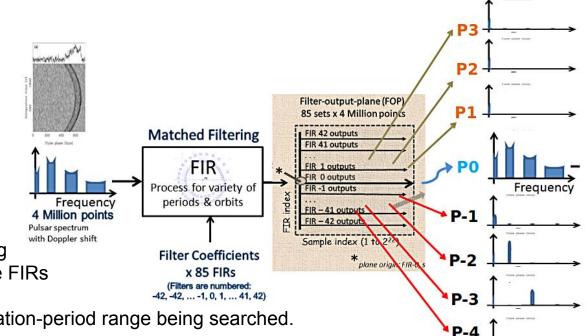
FDAS module receives RFI mitigated complex spectra generated from a dedispersed time-series.

Each spectrum is processed in a set of 84 matched filters

FIR filters used for Matched filtering FFT method used to implement the FIRs

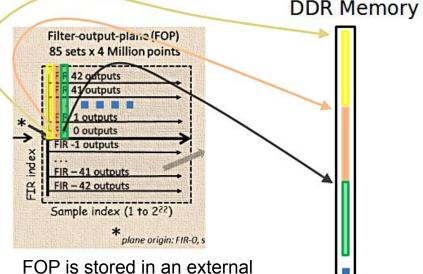
Each FIR probes a unique acceleration-period range being searched.

FIR outputs are detected and saved in a filter-output-plane (FOP) array FOP array is processed using a harmonic summing module



## 3.1 Design details - Filter output plane (FOP)

FOP is an intermediate product in the FDAS Stored as an array in the FPGA external memory FIR-numbers Vs Frequency-bins as row Vs Column of the FOP Array



memory in a column ordered manner so as to simplify the memory access duirng the harmonic summing.

# 3.1 Design details - Filter output plane (FOP)

FOP is an intermediate product in the FDAS Stored as an array in the FPGA external memory FIR-numbers Vs Frequency-bins as row Vs Column of the FOP Array

Outputs above a threshold is a detection

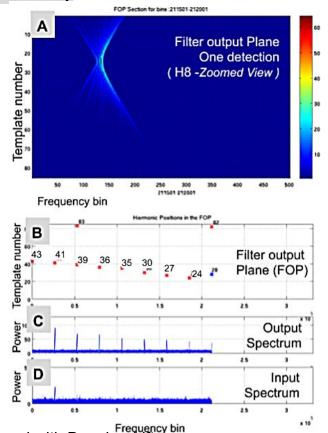
### **Unaccelerated Periodic signals & Harmonics**

- detections appear along FOP middle row

### **Accelerated Periodic signals & Harmonics**

- deconvolved by matched filters
- detections appear across the FOP
- positive acceleration along upper half of FOP
- negative acceleration along lower half of FOP
- A: view of the filter output plane around a harmonic position.
- B: FOP showing multiple (eight harmonics and a few spurious) detection.
- C: Recovered spectrum after the matched filtering.

D: Input spectrum shows only the fundamental and the higher harmonics are smeared with Doppler drift.



## 3.2 Design details - Harmonic Positions

A fundamental frequency being probed could be a non bin-centered frequency in the FOP and hence their higher harmonics are to be traced around a set of neighbouring bin positions.

Harmonics (2 to 8) of a non bin-centered fundamental will appear along (3 to 9) neighbouring bins.

To sum up to eight harmonics Total of 40 bin positions to be considered

#### (B+/-0.5)1 = b+/-0.5 <sup>556</sup> **1 Bin 3 Bins** (B+/-0.5)2 = 2b+/-1S 555 <u></u> 1110 -B 1 H2 554 1109 100 50 100 5 Bins (B+/-0.5)3 = 3b+/-1.53 Bins (B+/-0.5)4 = 4b+/-2.u 2220 2218 100 'n 50 100 (B+/-0.5)5 = 5b+/-2.5 2776 5 Bins (B+/-0.5)6 = 6b+/-37 Bins <u>§</u> 3330 2774 2772 3325 100 (B+/-0.5)7 = 7b+/-3.5 3886 7. Bins 9 Bins (B+/-0.5)8 = 8b+/-4<u>쫕</u> 4440 1 + 3 + 3 + 5 + 5 + 7 + 7 + 7 + 9 = 40

### (Quantized)

## 3.2 Design details - Acceleration Processing

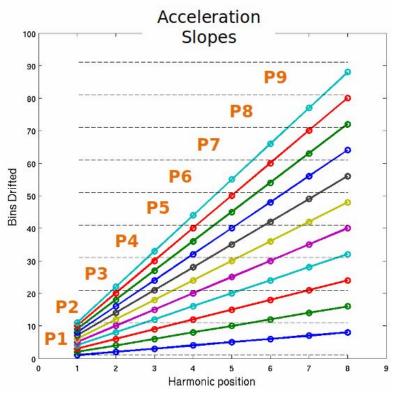
A complexity locating fundamental & harmonics in FOP

Accelerated signals and their harmonics can get deconvolved by different matched filters

Position of the harmonics will drift along the FOP rows.

Each filter deconvolves a narrow range of acceleration and frequency combination.

Acceleration processing is carried out across 11 steps.



# 3.2 Design details - Harmonic Summing

Summing fundamental & harmonics in the FOP is a complex task

Harmonic summing process should be able to

- Sum the harmonics along neighbouring frequency-bins,
- Sum fundamental and harmonics along the filter-rows
- Sum different harmonics from different filterrows

Harmonic summing module is realised by arranging the adders as illustrated in the Figure.

A simple logic to Sum the Harmonics

## 3.3 Design details - Firmware

- Industry partner M/s Covnetics Ltd, UK
- VHDL based design
- Modern FPGA Accelerator PCIe platform
- First implementation completed
- Design scaling through generics
- Diagnostic modes
- Early Power Estimates

# 3.4 Prototype implementation

Reduced version of FDAS

Implemented on a Bittware A10PL4 FPGA

Design consists of

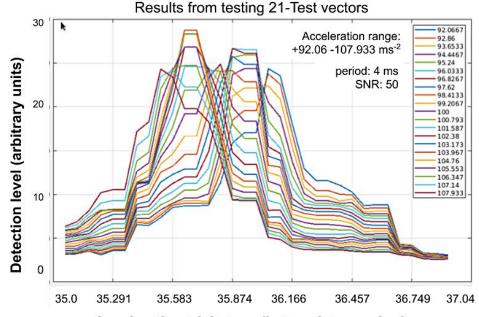
- Template matching with 85 FIRs
- Harmonic summing framework
- DDR4 memory banks for data storage

Meets the processing time estimates of 500 ms

Power consumption of about 35 W Match with Early Power Estimates (EPE)

## 3.5 Matched filtering results

- Test with fake pulsar data
- Range of test vectors used
- FOP generated by prototype
- Analysed for harmonic recovery using Matlab tools
- Significant match with reference



Acceleration trial steps (in template number)

Overlay of 21 result profiles from the prototype presented here. Acceleration cases between 92 and 108 m/s/s, period 4 ms and SNR 50 considered. The detections show peak values in the profiles and they shift (as expected) from the left to the right with accelerations changing from 107.9 to 92 m/s/s.

# 3.6. Future work and conclusion

### Future work

Several enhancements to FDAS considered

- 1. New feature harmonic summing to handle non-bin centred fundamentals
- 2. A Matlab model of new summing structure developed
- 3. Harmonic Suming enhancement to add up to 16 harmonics for the zero acceleration
- 4. Improvements to the user interfaces
- 5. Enhancement to FPGA configuration mechanisms for remote sites
- 6. Tests with real telescope data

### Conclusion

- 1. An FPGA Architecture developed to search for accelerated pulsars with SKA.
- 2. The design is based on a modern power efficient FPGA.
- 3. Prototype of the design with crucial functionalities implemented and tested
- 4. The template matching is fully functional
- 5. Upgrade options are being explored

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