Design and Development of a Wide-Field Fully Cryogenic Phased Array Feed for Arecibo

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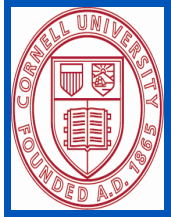
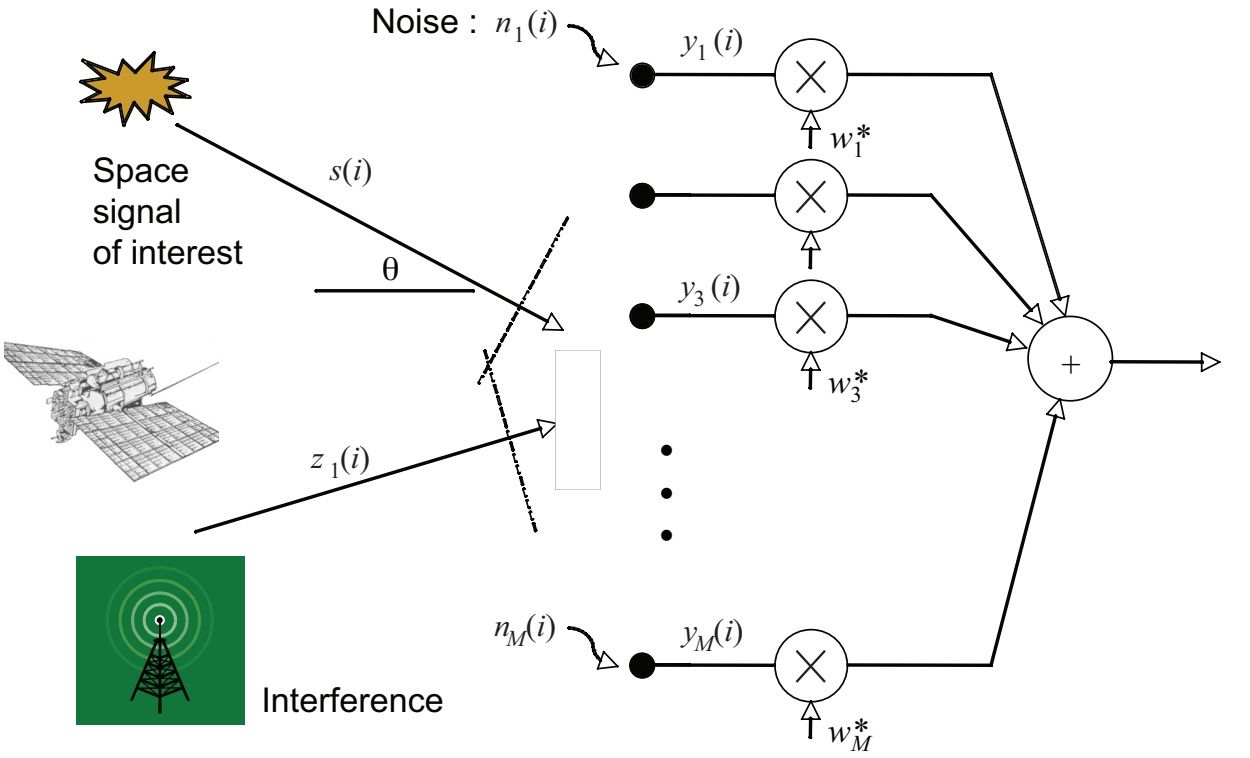


BYU Electrical & Computer Engineering
IRA A. FULTON COLLEGE OF ENGINEERING

ALPACA Grant Details

- NSF Award AST-1636645
- Brigham Young University, Cornell University, UCF
- 4 years, $5.8M
- Cornell: PAF front-end, including electronics, array elements, dewar, cryogenics, mechanical engineering
- BYU: Overall project management, signal downlink, digital beamformer, data handling
- UCF: Site preparation, installation and testing support.
- 2.5 year funding wait over!

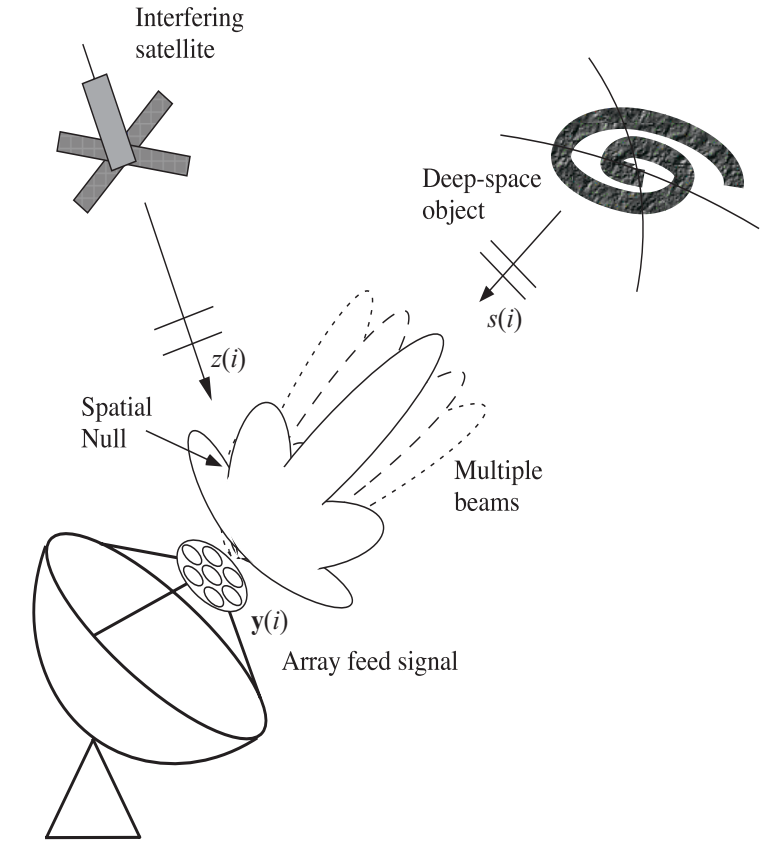
The PAF Narrowband Digital Beamformer



- Repeat for each frequency channel.
- $\mathbf{w}_k$ is frequency dependent.
- $\mathbf{w}_k$ steers beam mainlobe toward $s(i)$

Beamforming Capabilities

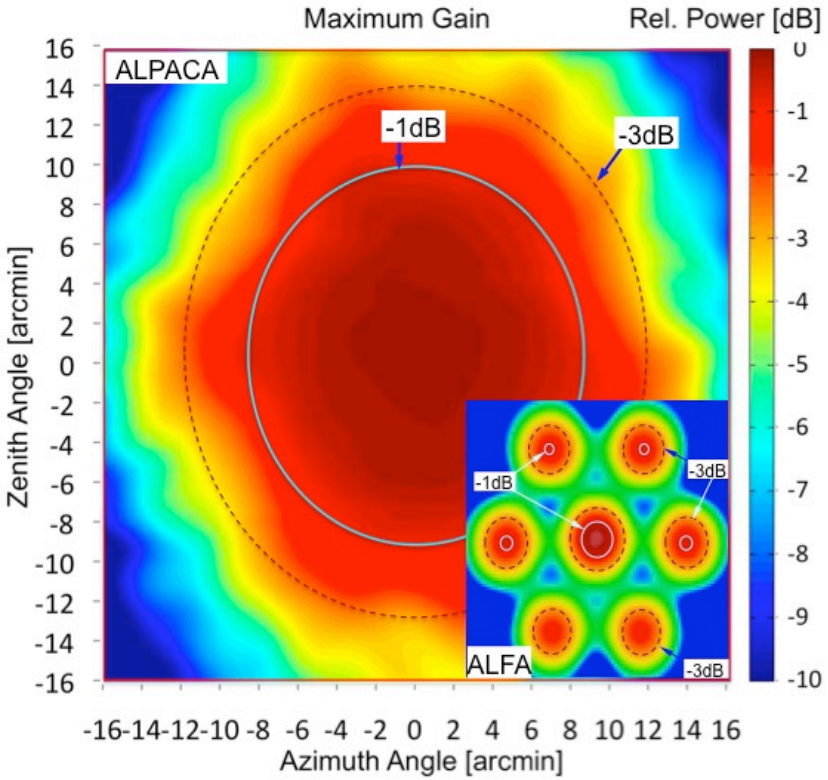
- Densely-packed simultaneous beams
- Fully sample the optics-imposed field of view
- Potential for adaptive spatial filtering to null RFI sources
- Potential for beampattern shape control to combat coma



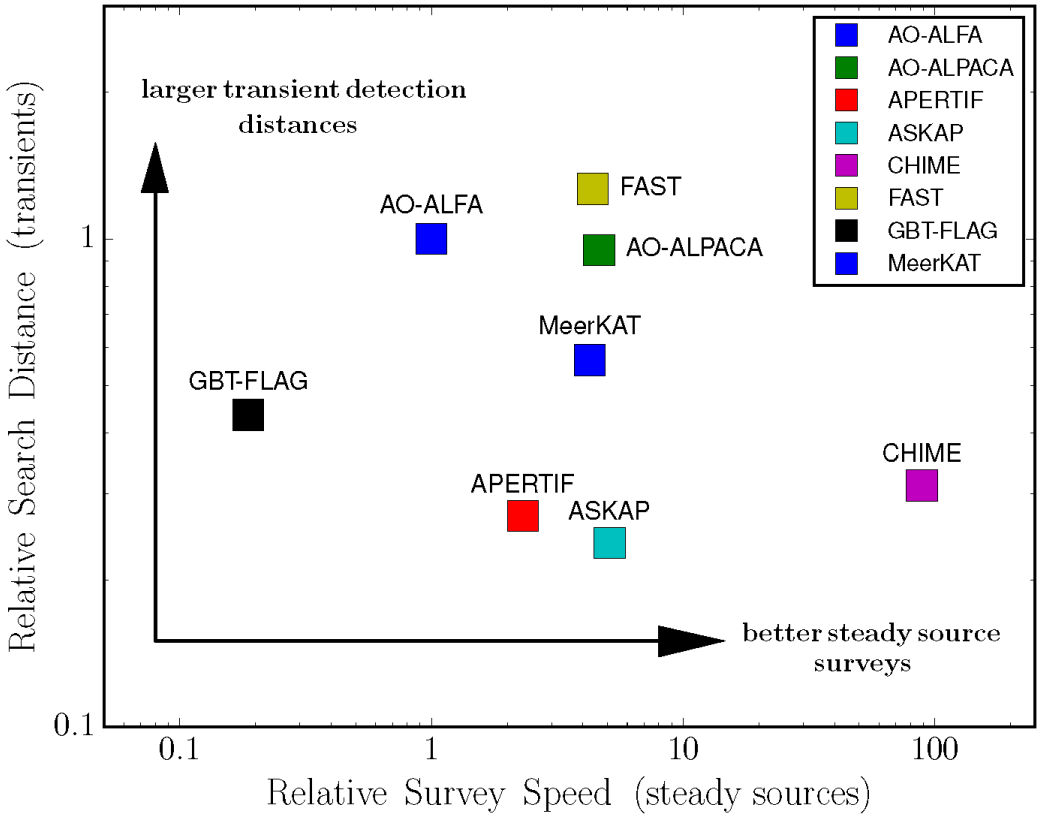
Radio telescope dish with a phased array feed

PAFS are all about survey speed and sky mapping

Field of view compared
to existing 7 beam ALFA receiver:



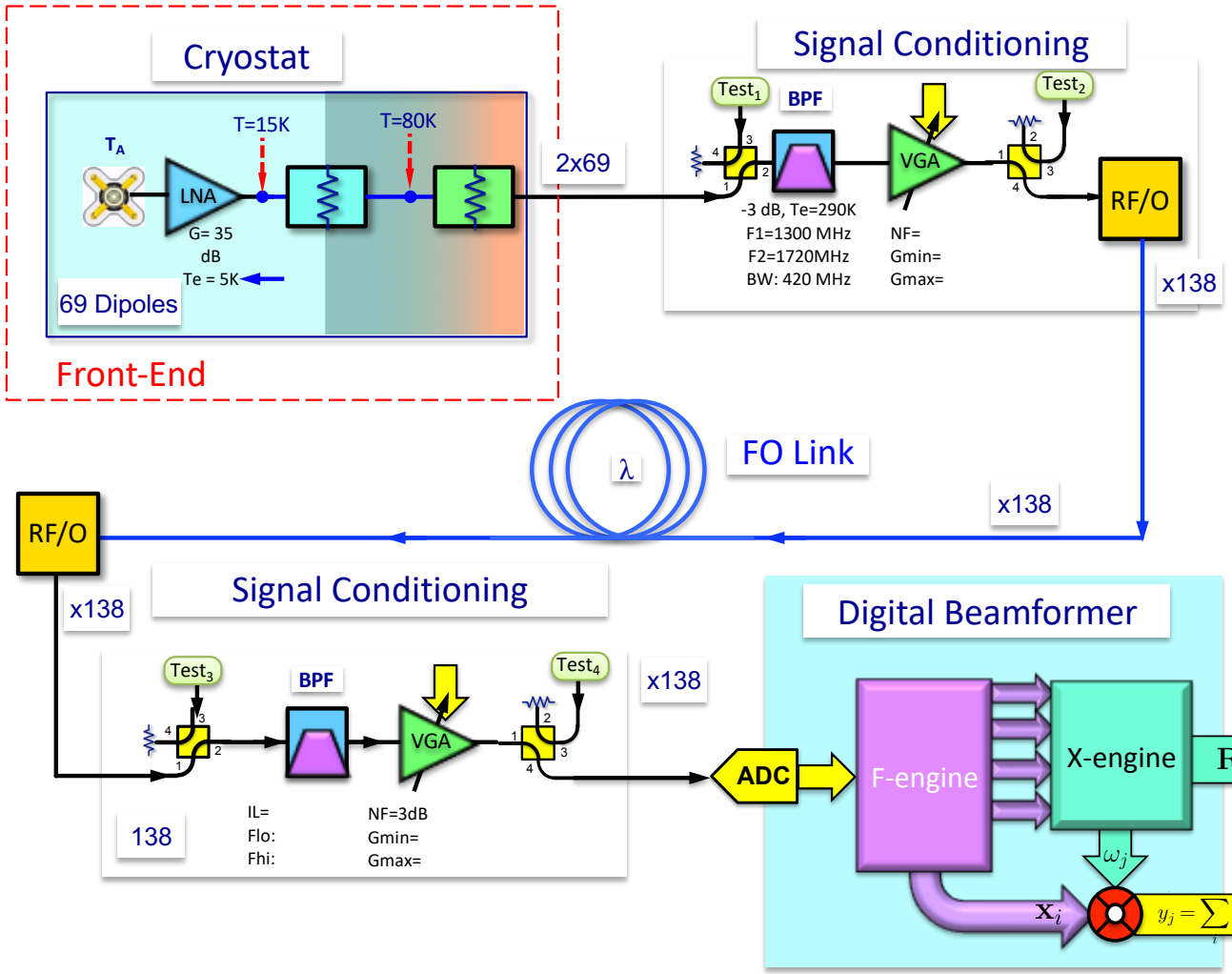
Performance compared to other astronomical receivers



Science Goals for ALPACA

- ALPACA design is targeted for:
  - HI and other long-integration, fine resolution spectral line observations
  - Pulsar/transient observation and parameter estimation
- Primarily a survey and mapping instrument due to wide field of view

ALPACA Cryo PAF
Architecture Rev Jun, 2019



ALPACA Performance Specs. (1)

Performance Characteristic	Specification
Frequency Coverage (tunable within this range)	1300 – 1720 MHz (420 MHz total BW)
Beamformer real-time processing bandwidth	305.2 MHz
Number of real-time beams	40
Integrated spectra data products per beam, per channel	XX pol (real float), YY pol (real float), XY pol (complex)
Pulsar / Transient mode:	
Number of frequency channels | BW per channel	1250 coarse chan. | 244.1 kHz separation, 325.5 kHz BW
Fastest integration dump interval	64 microseconds
HI Spectral Line (zoom spectrometer) mode:	
Total number of frequency channels | BW per channel	36,000 (spanning 183.7 MHz) | 5.1 kHz
Shortest integration dump interval	100 ms
Beamformer calibration mode:	
Covariance matrix outputs per each 512 coarse channel	Lower triangular 144x144 matrices, 500 ms max dump rate

ALPACA Performance Specs. (2)

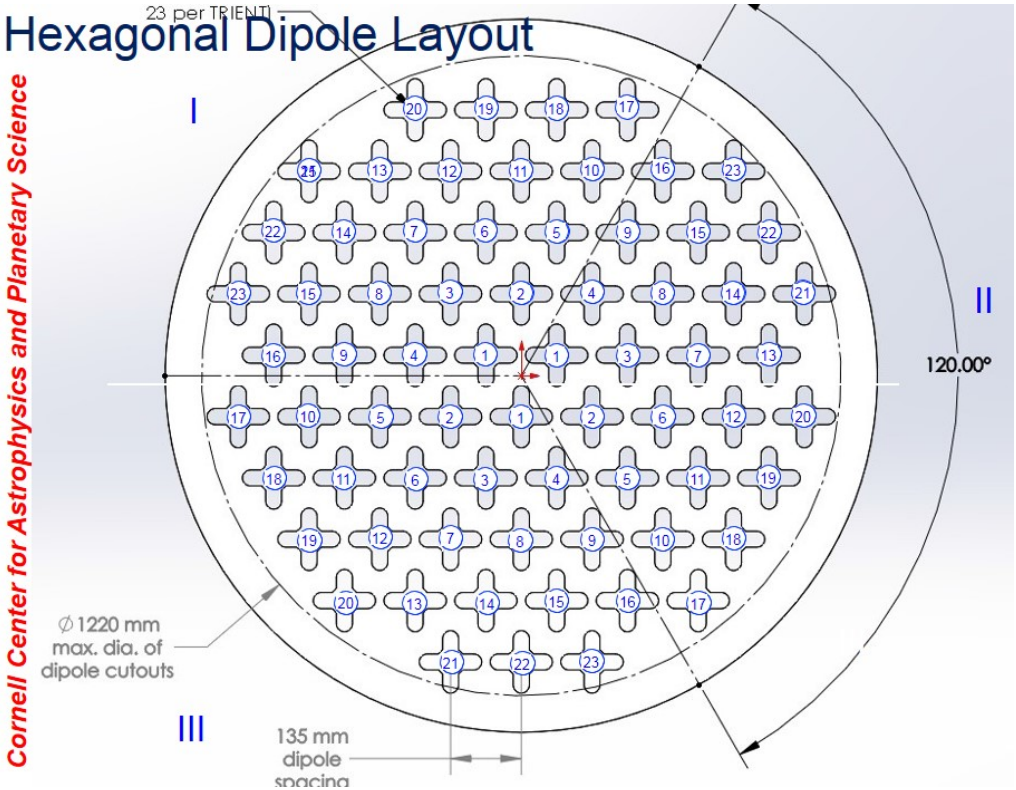
Performance Characteristic	Specification
LO and IF frequencies	NONE: direct sampling of bandpass RF
ADC sample rate | resolution	2,000 Msamp/s | 12 bits (10+ enobs)
Complex baseband sample rate	500 Msamp/s
1st stage PFB FFT length | oversample ratio	2048 channels | 4/3 oversampled
2nd stage (zoom) PFB length | oversample ratio	64, pruned to 48 non-overlapped channels | 1/1
Peak I/O data rates:	
Output data rate per FPGA board | input rate per HPC	52.1 Gbps | 37.5 Gbps (8 bit real + 8 bit imag. samples)
Total max output data rate in pulsar spectrometer mode	50.0 Gbps (16 bit int real & 32 bit int complex: 16r+16i)
Optional (unfunded) beamformed voltage data mode:	(Ability to support these modes is undetermined)
Beamformed raw voltages data rate, total over all HPCs	520.8 Gbps (cmplx int 16, 40 beams, X&Y pol)
Beamformed raw voltages data rate, one HPC	20.83 Gbps (cmplx int 16, 40 beams, X&Y pol)

ALPACA Performance Specs. (3)

Performance Characteristic	Specification
Number of input ports (antennas)	138 + 6 spare = 144, index: $0 \le j \le 143$
Number of Xilinx ZCU216 FPGA boards | fid index	9 | index: $0 \le p \le 8$, fid = p
Number of HPCs	25 index: $0 \le i \le 24$
Number of GPUs per HPC	2 index: $0 \le l \le 1$
Number of processing threads per GPU	1
xid index: identifies a unique GPU & hashpipe thread	xid = $q = 2i + l$, $0 \le q \le 49$
Frequency channels processed by qth xid	$k \in \{q, q + 50, q + 100, \cdots q + 1200\}$ for xid range of $0 \le q \le 49$. This implies the channel index range is $0 \le k \le 1249$.
Reduced bandwidth modes: total BW processed options	305.2, 244.2, 183.1, 122.1, or 61.0 MHz total BW (i.e., select and process any of 5, 61 MHz wide subbands)

Array Geometry

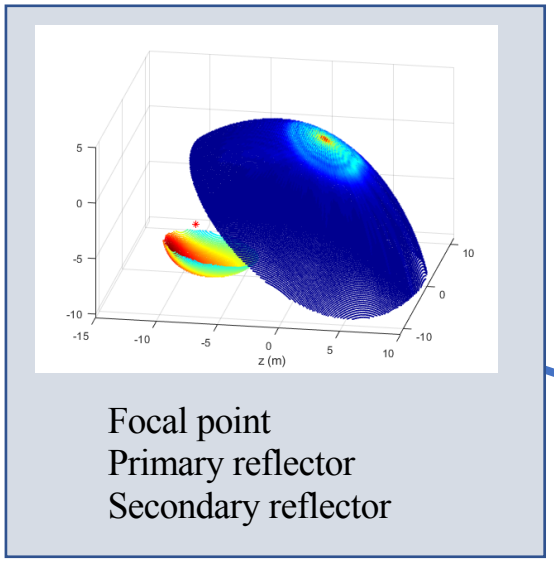
- Reduced component count
- Reduced processing requirements
- Similar FOV sensitivity flatness
- Improved T_{sys} due to lower mutual coupling and better impedance match
- Reduced cryogenic cooling complexity: 1 compressor, 3 cold heads vs 2 and 4 respectively

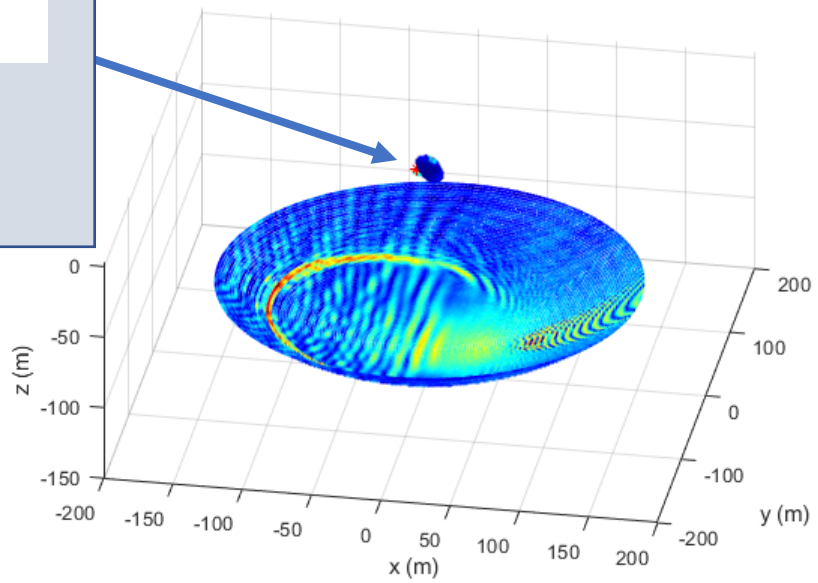


Simulation Model

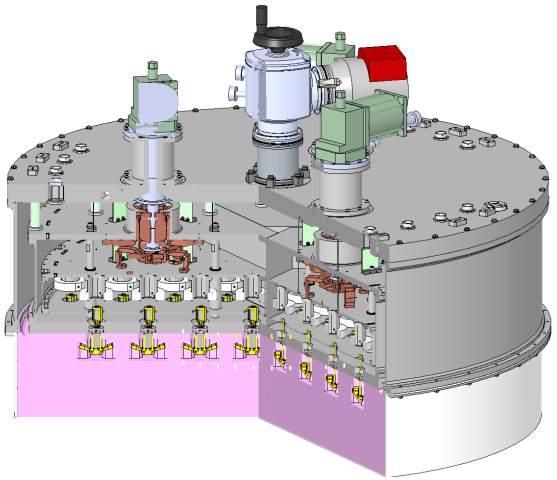
Model steps:

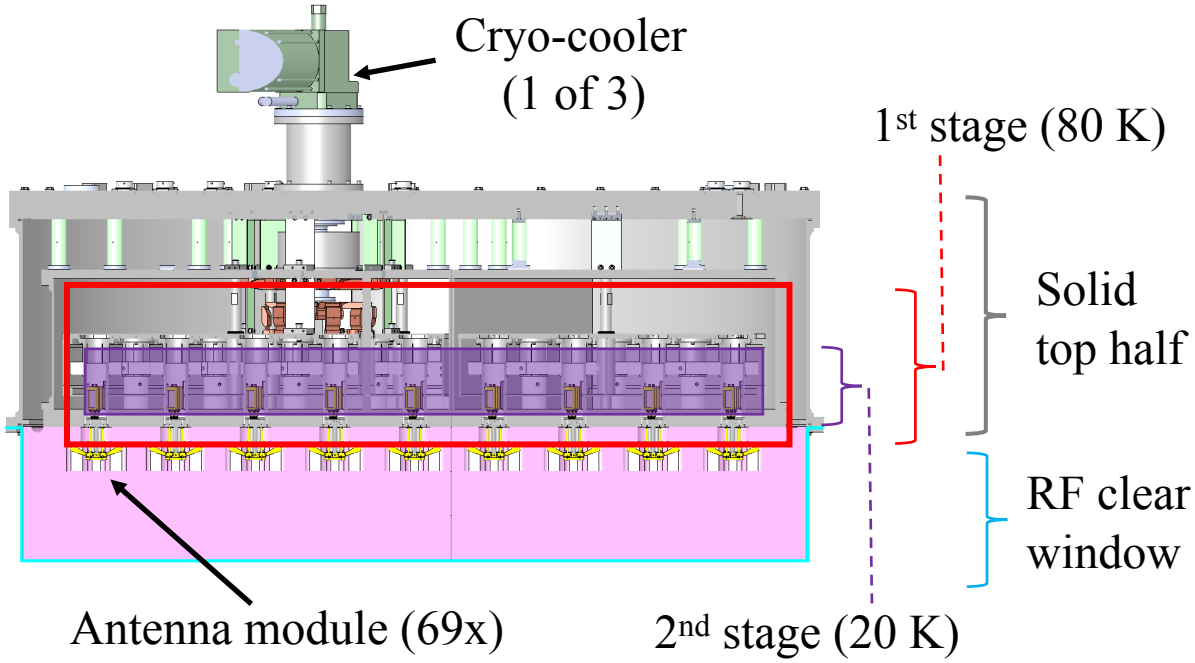
- Embedded element patterns (FEM, CST)
- Propagate to primary reflector
- Propagate to secondary
- Propagate to tertiary
- Propagate to far field
- Use reciprocity to determine received voltages at the element terminals for a plane wave incident on the primary reflector





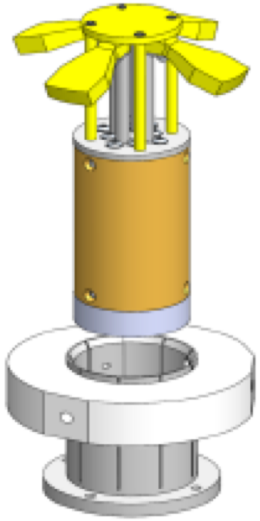
Cryostat Design





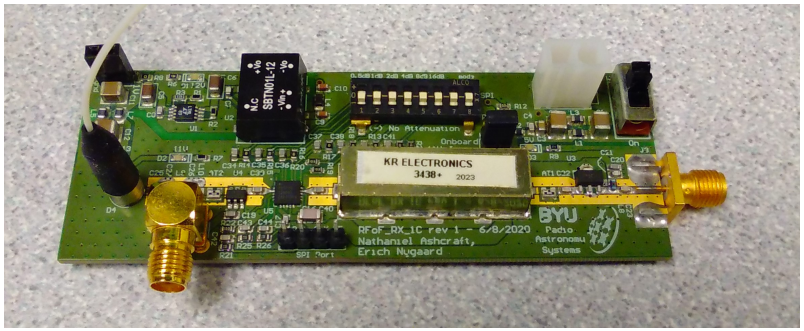
LNA + Dipole Module

Initial prototype design

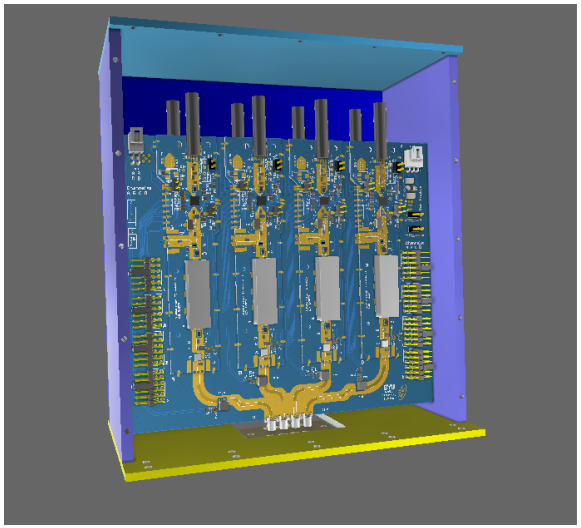


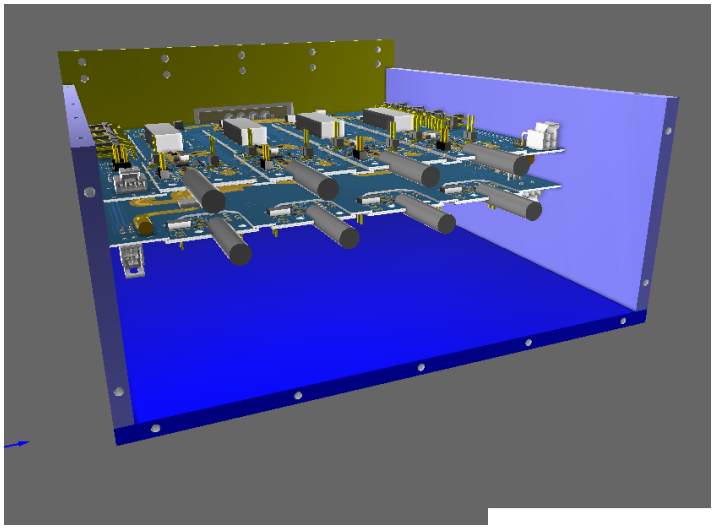
Final Design with Optimized Dipole Element

Signal Transport: RF over Fiber



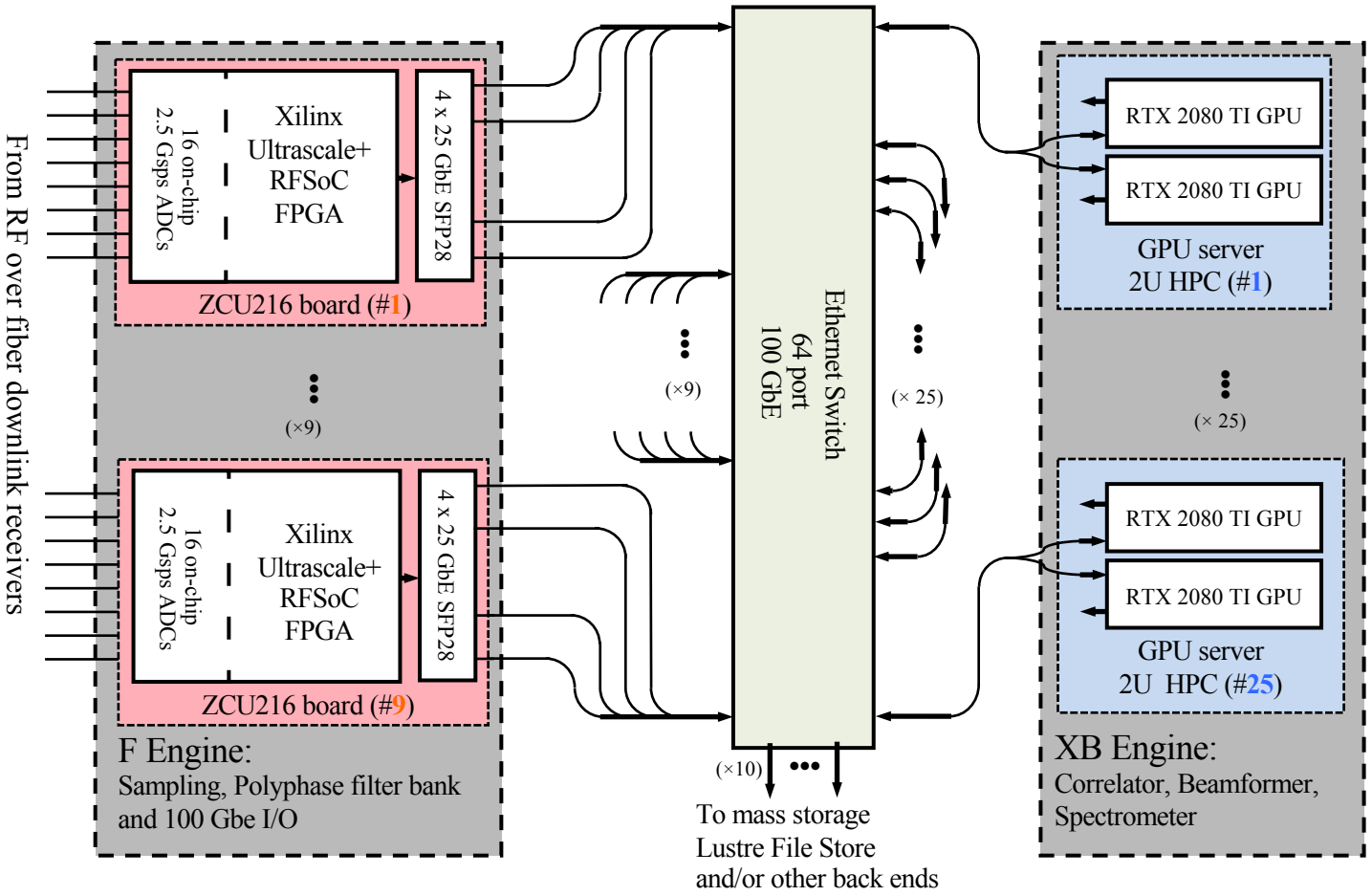
Single channel transmitter prototype design



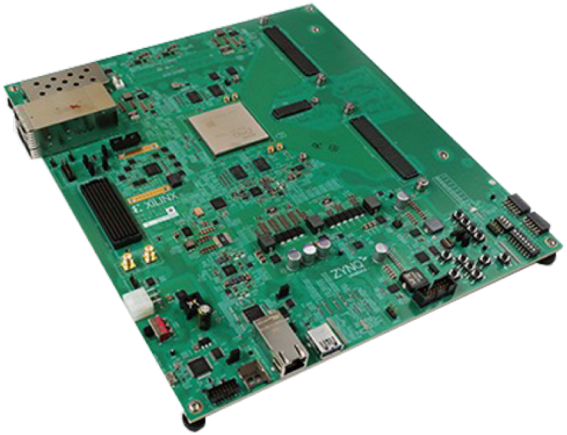


Design rendering for the 8-channel transmitter box that is mounted on the outside of the cryostat

Beamformer Subsystems

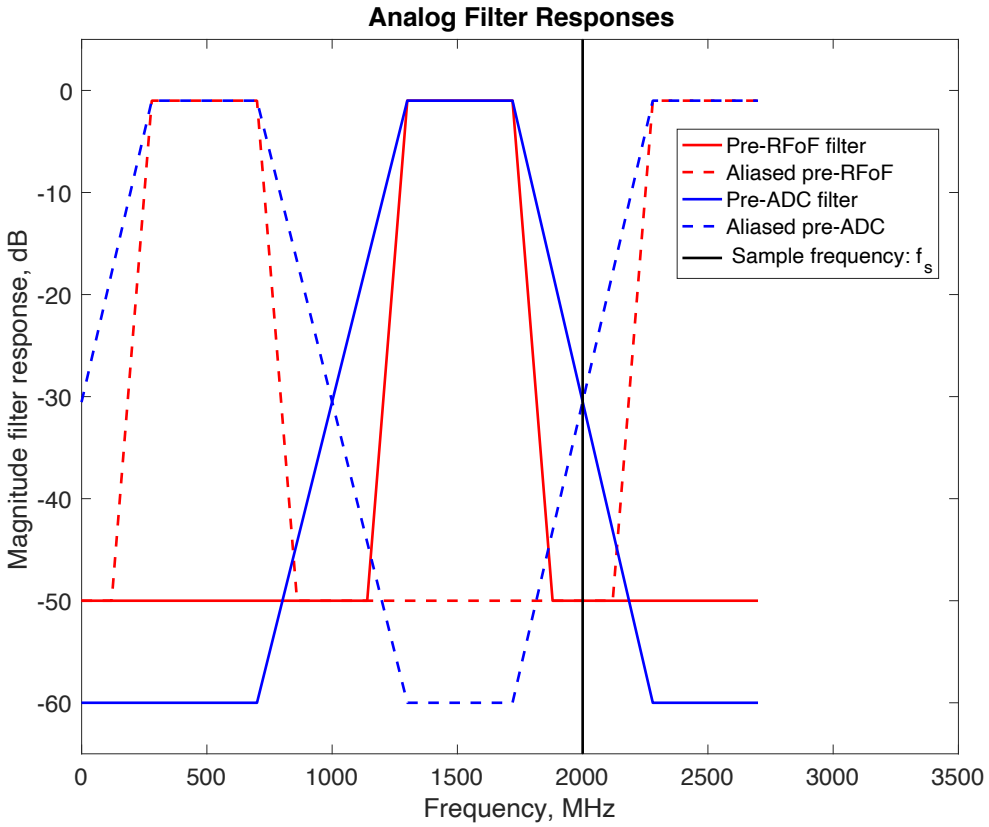


RFSoC F-Engine



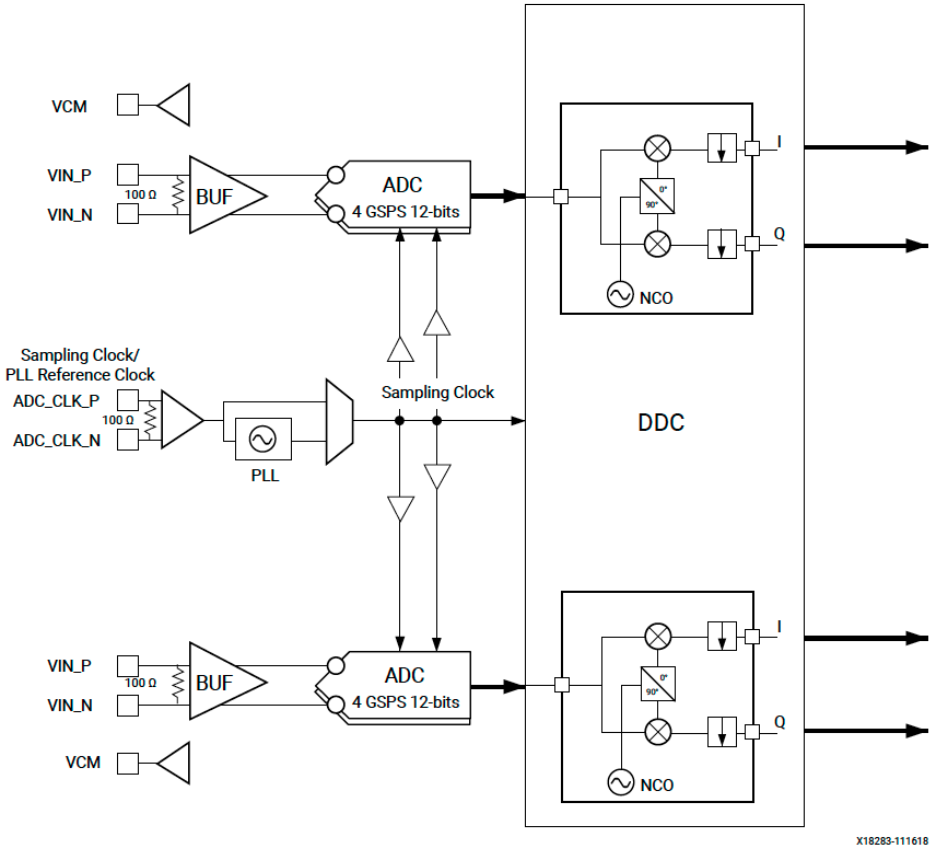
- XZCU49DR RFSoC has 16 on-chip ADCs, 2.5 Gsamp/sec, with digital down conversion and lowpass filtering to complex baseband
- Will directly sample RF over fiber downlinks with no analog mixer
- 4 x 25 GbE ports support I/O data rate to HPC/GPUs.
- 9 of these ZCU216 boards will be used to support 138 antenna inputs
- Oversampled polyphase filter bank for coarse frequency channelization

ADC, Sampling, and Pre-Filtering



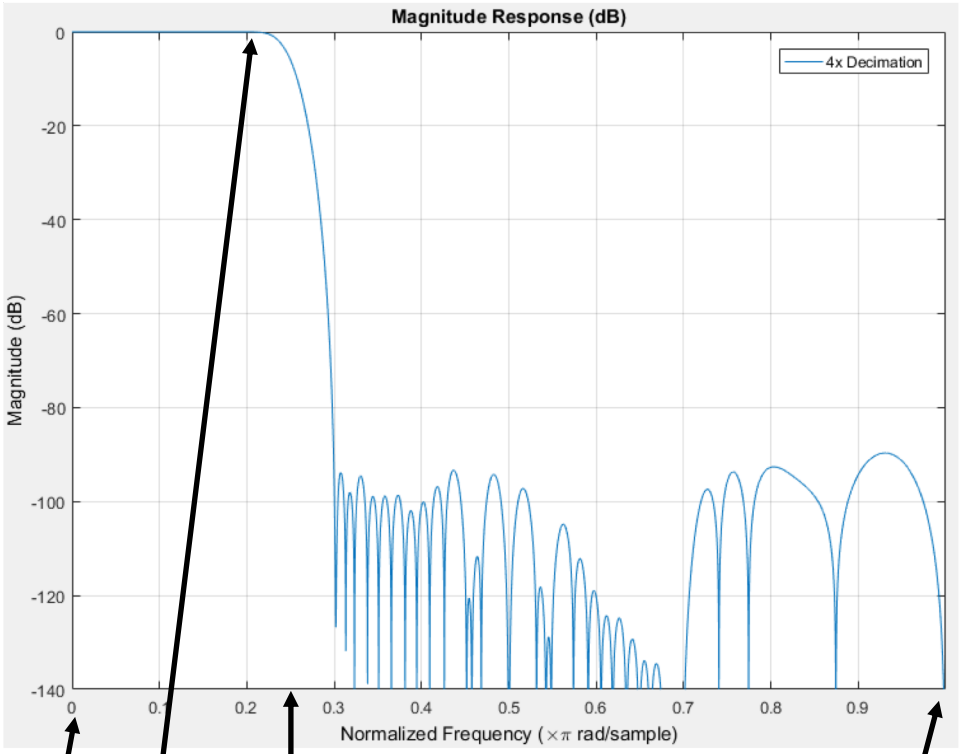
- Passband corners:
  1300 MHz to 1720 MHz
- Band-defining filter attenuates adjacent RFI prior to the RF over fiber link to limit dynamic range
- Anti alias filter is just ahead of ADC to reduce noise aliased into passband
- Pre-ADC filter is lower order, lower cost

ADC, Digital Down Conversion



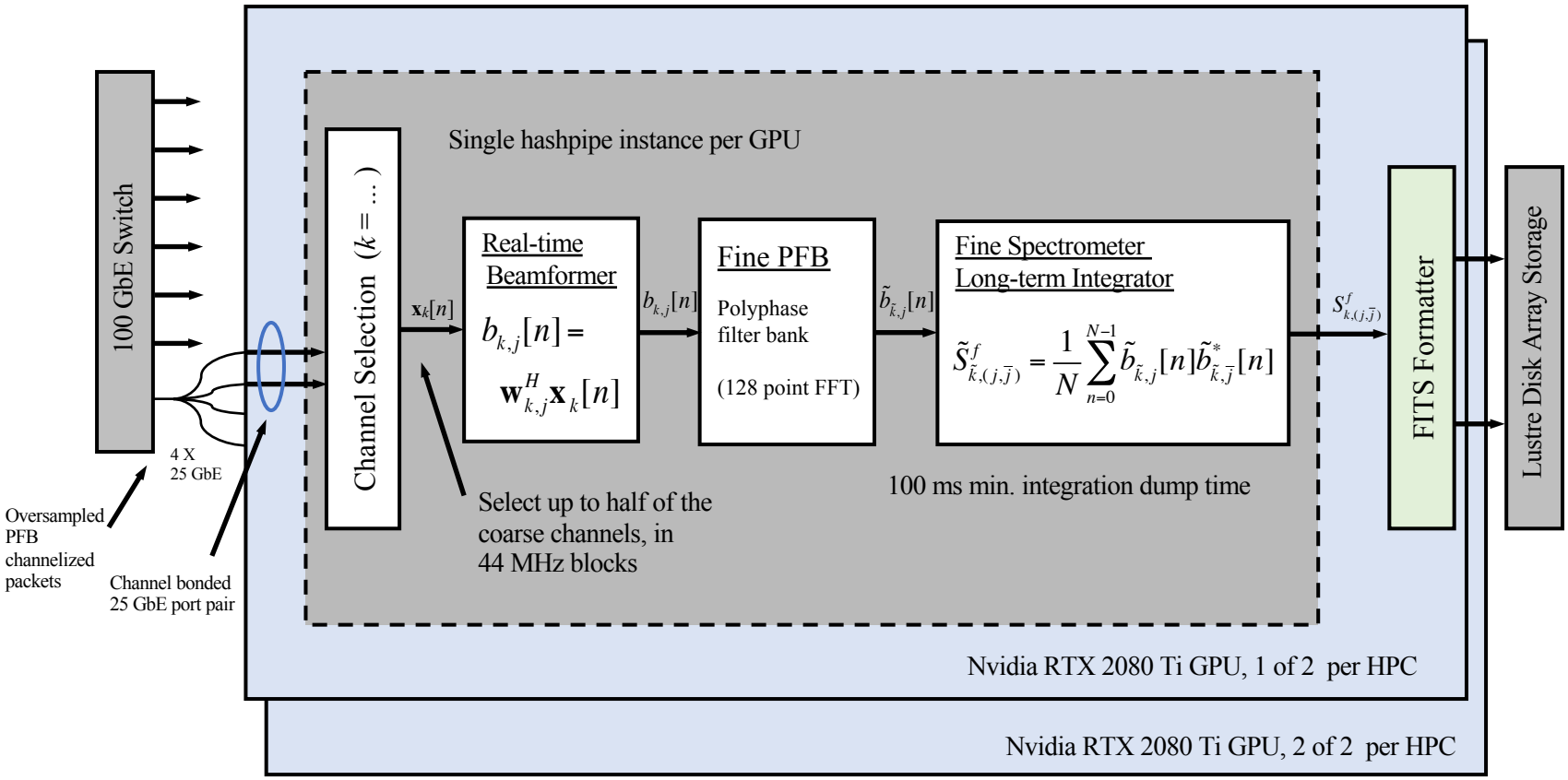
- Built-in ADC Digital Down Converter (DDC)
- 2 GHz sample frequency
- Mixes sampled real RF down to complex baseband
- Decimates to final sample rate of 500 MHz

ADC, Digital Down Conversion

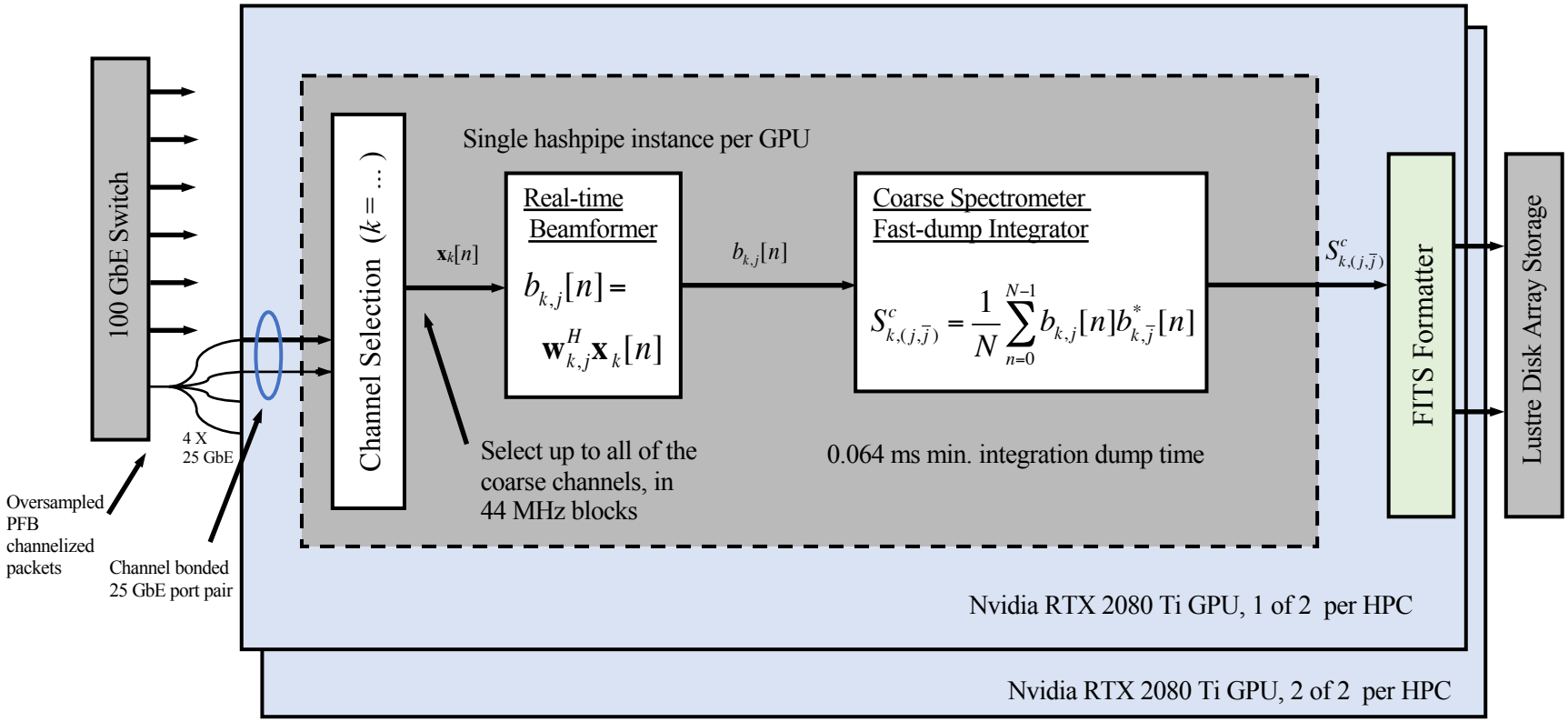


- Built-in ADC pre-decimation anti-alias filter response.
- Decimation by 4 moves. 250 MHz to full bandwidth point at 1.0.
- Complex baseband sample rate is 500 MHz.
- 420 MHz usable passband.
- No NCO tuning to select 305 MHz beamformer band: just pick from PFB channels.
- Ready for upgrade to 420 MHz beamformer with more HPCs.

HI Mode, Fine PFB (1 of 25 HPCs)



Transient Mode, Coarse PFB (1 of 25)



Beamformer Calibration Mode (1 of 25)