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FPGA architecture to search for accelerated pulsars with SKA

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Abstract

This paper presents a design which uses an FPGA (Field Programmable Gate Array) to search for radio pulsars in binary systems for the Square Kilometre Array (SKA). The search pipeline executes Doppler de-acceleration algorithm in real-time to identify binary pulsar spin periods. It involves a very large computation and the algorithm implementation for a real-time execution with power efficiency for the SKA is a challenging task. The design follows a Fourier domain acceleration search method, which is essentially a matched filtering technique, where the complex spectra of the dedispersed time-series are convolved with a set of Doppler demodulation templates. Convolution outputs are systematically summed over a number of harmonics and signatures of periodic signals are detected and passed on for subsequent downstream processing. This design is developed for modern FPGA technology and a prototype of the design is implemented and tested on a commercial FPGA accelerator platform. Salient details of the work are presented in the paper.

1 Introduction

Pulsar science is one of the key science drivers of the SKA telescope [1, 2, 3]. The binary pulsars are the jewel in the crown when it comes to testing the theories of gravity in the strong-field regime. However searching of the highly accelerated systems in relativistic binaries is one of the highly compute intensive (about 10 peta-OPS) tasks and a suitable high-performance computing solution is required for an implementation [4, 5].

The computational complexity for a pulsar search comes from several factors. The search needs to account for a range of distances, periods, binary orbits and deal with RFI [6]. The signals are quantized to multi-bit, observations are made across a very wide band of frequencies and the sky is simultaneously searched at more than 1000 directions (Fig.1). This paper presents a novel design developed to address this computational problem. The design is based on modern FPGA and a prototype was implemented and tested on a commercial accelerator platform.

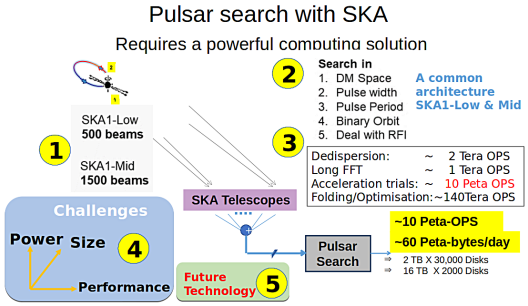

Figure 1. One full day of SKA Mid-frequency band-3 pulsar survey would generate about 60 petabytes of data requiring more than 10 peta-OPS computing power.

2 Design Philosophy

A search for pulsars in binary systems where the frequency is changed significantly during the observation can be undertaken in either the time or frequency domain. We have selected the later option and developed a new FPGA architecture to implement the Fourier domain acceleration search (FDAS) algorithm [7, 8]. Frequency changes caused by orbital motion over an integration time manifest in Fourier space as sinc functions convolved with an FIR response. The FDAS technique relies upon predicting the complex form and phase of the FIR filters and from this prediction, the frequency-reversed and complex conjugated templates for the matched filters are constructed (Fig.2). The templates are convolved with the respective Fourier bins to deaccelerate the input signals.

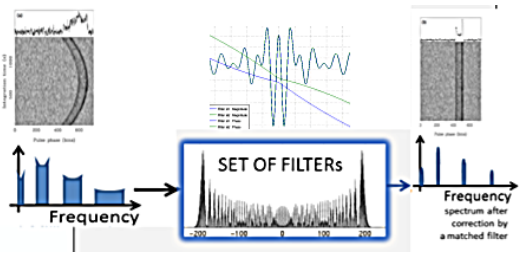

Figure 2. Matched filtering to deconvolve the Doppler induced accelerations.

A study into the Doppler induced response revealed that the conjugate filters can deconvolve the positive and negative accelerations simultaneously (Fig.3) and it can be exploited in the matched filter processing.

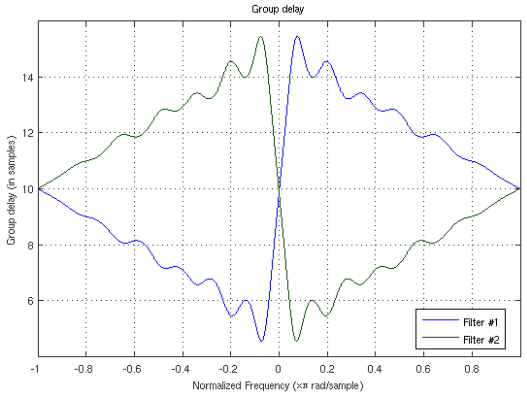

Figure 3. Conjugate coefficients are used in the matched filtering. The group delay between a positive and negative acceleration filter is shown in the figure.

3 Design details

The FDAS module receives RFI mitigated complex spectra generated from the dedispersed time-series. Each spectrum is processed in a set of 84 matched filters, with each filter probing a unique acceleration-period range being investigated in the search. An FFT based FIR simplified implementing the matched filters. The outputs from the filter are detected to obtain the power series and saved in a filter-output-plane (FOP) array.

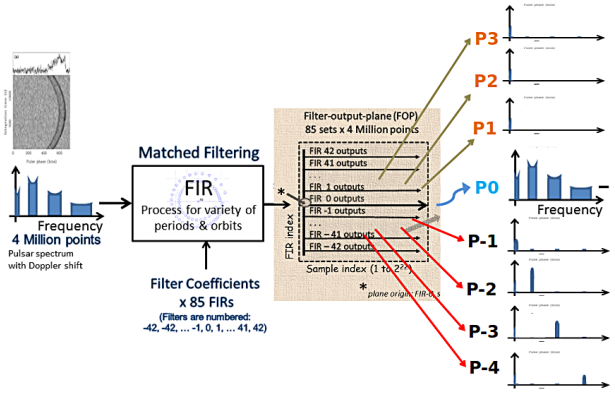

Figure 4. FDAS implementation. The main processing consists of matched filtering and harmonic summing in the filter output plane.

3.1 Matched filtering and Filter output plane

The FOP is an intermediate product in the processing and it is located in the FPGA external memory (Fig. 5) as an array with the filter-sequence and frequency-bin as indices. Unaccelerated periodic signals and their harmonics will appear in the middle of the FOP, which is regarded as the zero-acceleration row. Accelerated periodic signals and their harmonics would get deconvolved by the different matched filters and hence would appear across the FOP with a positive gradient at the upper half of the FOP or negative gradient at the lower half of the FOP (Fig.6B) based on the acceleration polarity. Matched-filter output power above a certain threshold is considered as a detection as indicated by the 'x' marks in Fig, 6A&B.

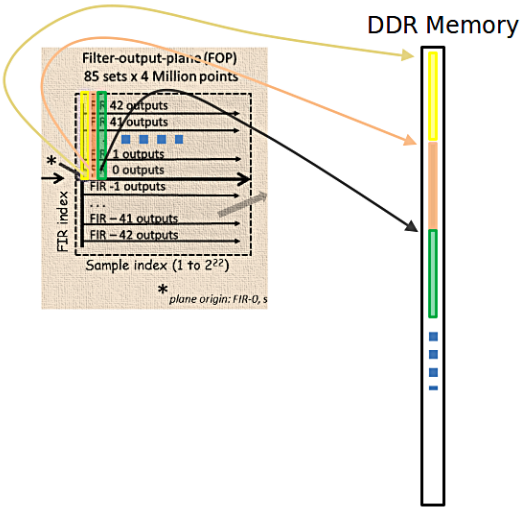

Figure 5. Memory access: The FOP is stored in the external DDR memory in a column ordered manner. This arrangement allows fetching data for the harmonic summing by a simple and linear memory read operation.

3.2 Harmonic summing

In the subsequent processing, a range of fundamental frequencies and their harmonics are verified through a harmonic-summing process in order to detect weak periodic signals. A fundamental frequency being probed could be a non bin-centered (in the power spectrum) frequency and hence their higher harmonics are to be traced around a set of neighbouring bin positions as indicated by Fig.7 subplots. In addition, if the signal is also accelerated then their harmonics get deconvolved only by a specific matched filter and hence the position of the harmonics will drift along the FOP rows. Yet another complexity in locating the fundamental and higher harmonic positions in the case of highly accelerated periodic signals is that they each can get deconvolved by different successive filters. However the slope of detection progress in terms of the filter number can be predicted depending on the acceleration as illustrated in Fig.8. Thus, the harmonic summing process should be able to 1) locate the harmonics along neighbouring frequency-bins, 2) locate the fundamental and harmonics along the filter-rows and 3) locate different harmonics along the different filter rows in the FOP. A basic harmonic summing process can be realised by arranging the adders as illustrated in Fig.9.

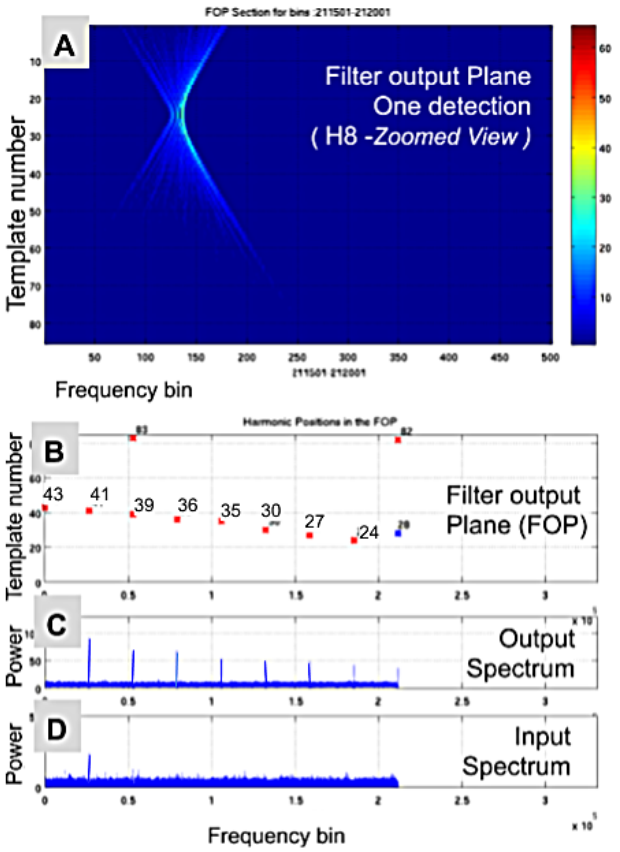

Figure 6. A: A view of the filter output plane around the eighth-harmonic position. B: Filter output plane showing multiple (eight harmonics and a few spurious) detection. C: Recovered spectrum after the matched filtering. D: Input spectrum. Only the fundamental is visible and the higher harmonics are smeared due to Doppler drift. In this illustration we have used the double pulsar test vector.

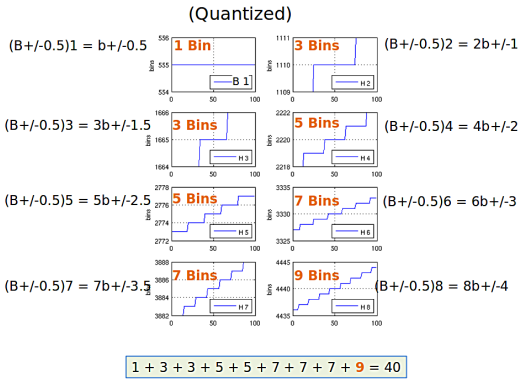

Figure 7. Harmonic positions: The harmonics of a non bin-centered fundamental will get positioned at the adjacent bin positions as indicated in the subplots. The legends 2-9 Bins indicate number of neighbouring bins that can register harmonic positions (2-8 harmonics) due to a non bin-centered fundamental (1 Bin). Calculations to arrive at the number of bin positions is shown next to each sub plot. A total of 40 bin positions is involved to sum up to eight harmonics.

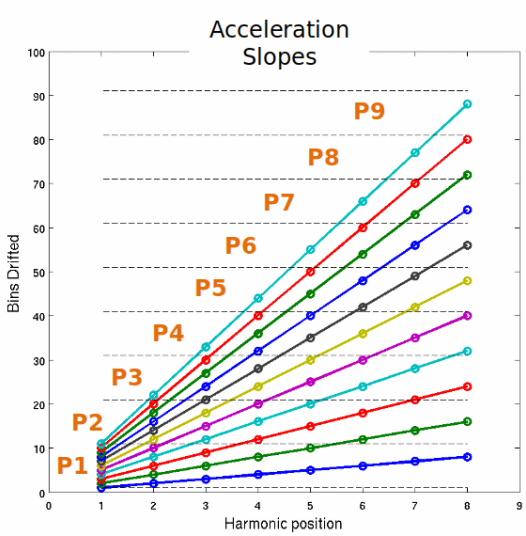

Figure 8. Acceleration processing is carried out across different steps. Figure illustrates an example case with eleven test signals, all of them having the same fundamental frequency (x=1) but different accelerations (y=1:11). The y-axis indicates the drifted frequency bin range that a given matched filter P1 to P9 is designed to deconvolve. The harmonics (x=2 to 8) of the signals are detected by different filters P1 to P9 depending on their acceleration. Each filter deconvolves a narrow range of acceleration and hence is able to detect more than one test signal, which is more obvious at the lower harmonics. For example, for the acceleration cases considered, the P1 filter is able to detect all eleven fundamentals, five 2nd harmonics, three 3rd harmonics and so on.

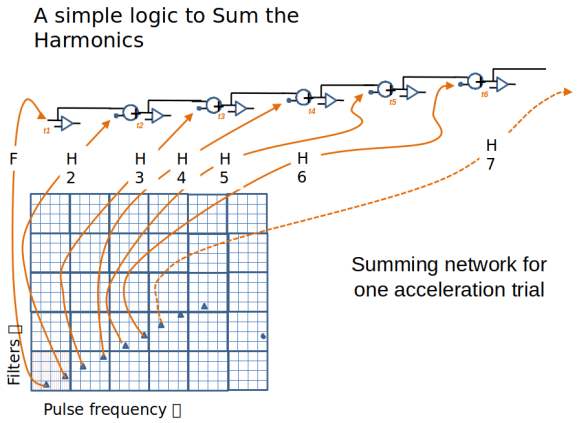

Figure 9. Harmonic Summing: An illustration for the adder network required to sum the harmonic positions.

3.3 Firmware design

A firmware design for the proposed FDAS architecture was taken up along with an industry partner M/s Covnetics Ltd, UK [10, 11]. A versatile firmware design that can be scaled to larger FPGAs and modern accelerators was realized. A configurable design was achieved through the use of generics introduced at the top level of the VHDL design. The generics are first optimally adjusted before the FPGA-design-synthesis operation to meet specific hardware configurations. The overall design can be easily configured to optimize the processing performance. The firmware operational modes are controlled through a PCIe interface.

The firmware also supports diagnostic modes. Normally, the FOP generated after the matched filtering is subsequently processed internal to the FPGA to perform the harmonic summing. However, the firmware allows a special mode to read the FOP by the host via the PCIe interface. This feature is of much use in systematically testing the FDAS. Similarly, firmware functions are available to read and verify templates and internal configuration registers in the FPGA. Also the FPGA operations can be executed in a single-stepping mode for any detailed diagnostic operation.

3.4 Prototype implementation

A reduced version of the FDAS firmware is implemented on a Bittware A10PL4 FPGA board. The design is based on the requirements and architecture specification as outlined in our design documents [10, 11]. The implementation consists of a template matching module and a framework for the harmonic summing. The template-matching module makes use of two DDR4 modules that are available in the A10PL4 board. The template matching is achieved using a 1024-point FFT based convolution network that processes 85 templates in six iterations. The harmonic summing section is configured to implement one simple summer module to test the basic detection process. The summer module is integrated to use one DDR4 memory to process the FOP data.

The time required to process one (DM) data set (sum of the template matching time and the harmonic summing time) is estimated to be 500 ms [10], which adequately meets the target specification for this implementation. The power consumed by the prototype FPGA design to execute the FDAS functions is about 35 W, which is significantly close to the early power estimates that we have made for the design.

3.5 Matched filtering results

We have extensively tested the prototype FDAS using fake pulsar test vectors. A range of test vectors covering different periods, accelerations and signal strength was generated and fed to the prototype to execute the matched filtering. After the processing, the FOP generated in the FPGA was readout and analysed for integrity and harmonic recovery using Matlab tools. The FPGA results are found to match very well with the Matlab reference analysis. A result from this analysis is presented in Fig.10.

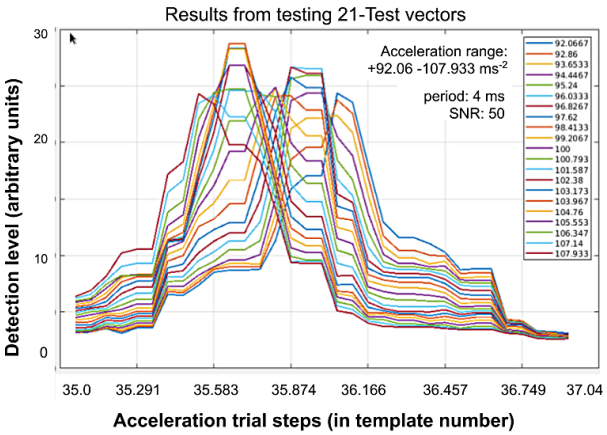

Figure 10. An overlay of 21 result profiles from the prototype is presented here. We have considered test vectors with acceleration between 92 and 108 m/s/s, period 4 ms and SNR 50. The FOPs produced after the matched filtering in the FPGA is analysed through Matlab to sum the harmonic positions. The detection level peak in the profiles shifts from left to right with the change in the test vector acceleration from 107.9 m/s/s to 92 m/s/s indicating the proper functioning of the matched filtering.

3.6 Future work

As a next phase in this work, we are considering several enhancements. Among those, a significant improvement is related to implementing and testing a new feature summing tree. Our existing summing tree structure in the FDAS adds along the vertical paths except at the edge bins. The enhancement that we consider here is meant to capture the drifted bin positions arising from non-bin centred fundamentals in a way that at least one of the available summing paths is able to sum along the expected drifted path. A Matlab model for this new summing structure has been developed and extensively verified with the test data. Incorporating this new feature will use additional FPGA resources, especially the DSP blocks and internal memory resources. The currrent prototype design sums upto eight harmonics. We are also exploring possibilities to enhance it to sum 16 harmonics for the zero acceleration (middle) row of the FOP. Apart from these, we are also considering improvements to the user interfaces and to the FPGA configuration methods to enable enhanced testing of the hardware in remote sites.

4 Conclusion

We have developed an FPGA Architecture to search for accelerated pulsars with SKA. The design is based on a modern power efficient FPGA. A prototype of the design with crucial functionalities have been implemented and tested

with a variety of test cases. The template matching part of the FDAS design is fully functional and future upgrade options are being explored. We will also be testing the deign with telescope data and at field environment in the very near future.

5 Acknowledgements

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